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FORM PTO-1449

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INFORMATION DISCLOSURE STATEMENT

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ATTY. DOCKET NO.
SP088.C6

APPLICATION NO.
10/083,143

APPLICANT
Deosaran et al.

FILING DATE
February 27, 2002

APPLICATION NO.
10/083,143

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	AB1	4,67	5,806	06/19	987	Uchi	da DECEIVED	364	200	
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	AF1	4,90	3,196	02/19	990	Pomer Packanology Center 210		<b>(</b> )864	200	
	AG1	4,94	2,525	07/19	990	Shintani et al.		364	200	•
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	AO	1	Agerwala, T. pp. 1-61 (Mar			jh Per	formance Reduced Instruction S	Set Processo	rs," IBM Res	search Division,
	АР	<u>1</u>	Aiken, A. and ESOP, Spring	Nicola ger-Ve	au, A., "Perfe rlag, pp. 221	ect Pip -235 (	elining: A New Loop Paralleliza 1988).	tion Techniqu	ue," <i>Proceed</i>	lings of the 1988
	AQ	<u>1</u>	Charlesworth 164 Family,"	, A.E., Compu	"An Approac	ch to S	Scientific Array Processing: The pp. 18-27 (September 1981).	Architectural	Design of the	ne AP-120B/FPS-
unt	AR	<u>1</u>	Colwell, R.P. Conference o (October 198	n Arch	"A VLIW Arc nitectural Sup	chitecti oport fo	ure for a Trace Scheduling Com or Programming Languages and	piler," <i>Proce</i> d Operating S	edings of the Systems, AC	e 2nd Internationa M, pp. 180-192
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1	AB2	5,10	9,495	04/19	92	Fite	et al.DECEN/EF	395		375		
	AC2	5,14	2,633	08/19	92	Mur	ray ela EUEIVEL	395		375		
·	AD2	5,16	7,026	11/19	92	Mur	ray et al. JUL 0 8 2002	395		375		
	AE2	5,21	4,763	05/19	93	Blai	ner et al.	395		375/		
	AF2	5,22	2,244	06/19	93	Car	bine <b>Fechnology Center 2</b>	<b>395</b>	/	800		
	AG2	5,22	6,126	93	Mcf	arland et al.			375			
V	AH2	5,23	0,068	07/19	93	Var	Dyke et al.	395		375		
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	AO	<u>2</u>					rcolation of Code to Enhance Pa pp. 1411-1415 (December 1971)		ispatc	hing and Exe	ecution," <i>IEEE</i>	
	AP	<u>2</u>					Scheduling and Register Allocati M, pp. 442-452 (1988).	on in La	arge B	asic Blocks,	" International	
	AQ	<u>2</u>					timizing Delayed Branches," <i>Pro</i> 0 (October 5-7, 1982).	ceeding	s of th	ne 5th Annua	al Workshop on	
rent	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," Proceedings 1989  IEEE International Conference on Computer Design: VLSI in Computers and Processors, IEEE, pp. 134-137 (October 1989).											
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	AB3	5,26	1,071	11/19	93	Lyor		395	425				
	AC3	5,27	8,963	01/19	94		ersley TOELVE	395 395	400				
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	AE3	5,34	5,569 09/19		94	Tran		395	375				
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bent	AN	<u>3</u>	Horst, R.W. & Annual Intern	t al., "I ationa	Multiple Insti	ructio on C	n Issue in the NonStop Cyclone Computer Architecture, IEEE, pp	Processor," . 216-226 (1	Proceedings 990).	of the 17th			
	AO	<u>3</u>	Hwu, W-M. W IEEE Trans. (	I. and On Coi	Patt, Y.N., "( mputers, IEE	Checl E, Vo	kpoint Repair for High-Peforman bl. C-36, No. 12, pp. 1496-1514	ce Out-of-O (December	rder Executio 1987).	n Machines,"			
	AP	3					oloiting Parallel Microprocessor Annual Symposium on Compute						
	AQ	<u>3</u>					High Performance Restricted D 4-13, IEEE, pp. 297-306 (June 2		hitecture Hav	ring Minimal .			
AR 3 IBM Journal of Research and Development, IBM, Vol. 34, No. 1, pp. 1-70 (January 1990).													
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Valna F	AA4		8,705	09/19	95	Ng	uyen et al.	395		3/5				
1	AB4	5,48	7,156	01/19	96		pescu et al.	395		375				
	AC4	5,49	7,499	03/19	96	Ga	ırg <i>et al</i> .	395		800				
	AD4	5,52	4,225	06/19	96 Kr		anich	395		403				
	AE4	5,56	0,032 09/19		96	Ng	uyen & RECEIVEL	395		800				
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bens	AN	4	Johnson, M. S	Supers	scalar Microp	oroc	essor Design, Prentice-Hall, Entir	e book si	ubmit	ted (1991).				
	AO	4	Johnson, W.	M., Su	per-Scalar F	Proc	essor Design, (Dissertation), 134	pages (1	989).					
	АР	4	Machines," P.	госеес	lings of the 3	3rd I	able Instruction-Level Parallelism International Conference on Archit ACM, pp. 272-282 (April 1989).							
	AQ	4		Jouppi, N.P., "Integration and Packaging Plateaus of Processor Performance," International Conference of Computer Design, IEEE, pp. 229-232 (October 1989).										
Went	AR	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," <i>IEEE Transactions on Computers</i> , IEEE, Vol. 38, No. 12, pp. 1645-1658 (December 1989).												
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hemo	AA5	5,60	6,676	02/19	97	Gro	chowski <i>et al</i> .	995	586				
	AB5	5,619	9,668	04/19	97	Zaio	di .	395	376				
	AC5	5,62	5,837	04/19	97	Pop	escu et al.	395	800				
	AD5	5,62	7,983	05/19	97		escu et appoint	205	393				
	AE5	5,70	08,841 01/199		/1998 Pop		escu et al. ILCLIV	255	800				
	AF5	5,73	37,624 04/199		98		g et al.	395	800:23				
	AG5		68,575 06/199				anano et ai.	395	569				
V	AH5	<del> </del>	5,778,210 07/19			Hen	escu et al.	2960	394				
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rns	AN	<u>5</u>	Keller, R.M., '	'Look-	Ahead Proce	esson	s," Computing Surveys, ACM, Vo	l. 7, No. 4, p	p. 177-195 (C	December 1975).			
	AO	5	Lam, M.S., "Ir Vol. 4, pp. 173			ng Fo	or Superscalar Architectures," <i>An</i>	nu. Rev. Co	mput. Sci., Aı	nnual Reviews,			
	AP	<u>5</u>	Lightner, B.D. - March 1, 199		lill, G., 'The	Meta	flow Lightning Chipset", Compcor	n Spring 91,	IEEE, pp. 13	-18 (February 25			
	AQ	<u>5</u>	Murakami, K. et al., "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," <i>Proc. 16th Int. Symp. on Computer Architecture</i> , ACM, pp.78-85 (June 1989).										
KINT	AR	<u>5</u>	Patt, Y.N. et al., "Critical Issues Regarding HPS, A High Performance Microarchitecture", <i>Proceedings of 18<sup>th</sup> Annual Workshop on Microprogramming</i> , IEEE, pp. 109-116 (December 3-6, 1985).										
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	AB6	<del>1                                    </del>	2,205	11/19	98	Kelly	retal.	395	185.06					
	AC6	5,83	2,293	11/19	98	Pope	escu et al.	395	800-23					
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	AO	<u>6</u>	Patterson, D. Publishers, p				Computer Architecture: A Quantit 1 449 (1990).	ative Approa	ach, Morgan I	Kaufmann				
	АР	<u>6</u>					nds in Microprocessors: Out-of-0  ", IEEE, pp. 263-266 (1991).	Order Execu	tion, Specula	tive Branching				
·	AQ	<u>6</u>	Pleszkun, A.R. and Sohi, G.S., "The Performance Potential of Multiple Functional Unit Processors," <i>Proceedings of the 15th Annual Symposium on Computer Architecture</i> , IEEE, pp. 37-44 (June 1988).											
wint	AR  6  Pleszkun, A.R. et al., "WISQ: A Restartable Architecture Using Qu u s," Proceedings of the 14th International Symposium on Computer Architecture, ACM, pp. 290-299 (June 1987).													
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Page 7 of 12 APPLICATION NO. ATTY. DOCKET NO. SP088.C6 10/083,143 **ORM PTO-1449** APPLICANT Deosaran et al. N DISCLOSURE STATEMENT GROUP FILING DATE February 27, 2002 **U.S. PATENT DOCUMENTS EXAMINER** CLASS SUB-**FILING DATE** DATE NAME INITIAL **DOCUMENT** NUMBER CLASS AA7 AB7 AC7 AD7 AE7 AF7 AG7 AH7 AI7 **FOREIGN PATENT DOCUMENTS EXAMINER DOCUMENT NUMBER** DATE COUNTRY **CLASS** SUB-TRANSLATION INITIAL CLASS AJ7 AK7 AL7 AM7 OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Popescu, V. et al., "The Metaflow Architecture", IEEE Micro, IEEE, Vol. 11, No.3, pp. 10-13 and 63-73 (June AN 7 bent 1991). Smith, M.D. et al., "Boosting Beyond Static Scheduling in a Superscalar Processor," International Symposium on AO 7 Computer Architecture, IEEE, pp. 344-354 (May 1990). Smith, J.E. and Pleszkun, A.R., "Implementation of Precise Interrupts in Pipelined Processors," Proceedings of ΑP <u>7</u> the 12th Annual International Symposium on Computer Architecture, IEEE, pp. 36-44 (June 1985). Smith, M.D. et al., "Limits on Multiple Instruction Issue," Computer Architecture News, ACM, No. 2, pp. 290-302 AQ <u>7</u> (April 3-6, 1989).

Sohi, G.S. and Vajapeyam, G.S., "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," Conference Proceedings of the 14th Annual International Symposium on Computer Architecture, pp. 27-34 (June 2-5, 1987).

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	AP	<u>8</u>	Tjaden, G.S a (Dissertation)				ntation and Detection of Concurr	ency Using (	Ordering Mat	rices,					
"	AQ	<u>8</u>	Tjaden <i>et al.</i> , Vol. C-22, No	Tjaden et al., "Representation of Concurrency with Ordering Matrices," IEEE Transactions On Computers, IEEE, Vol. C-22, No. 8, pp. 752-761 (August 1973).											
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